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Search Results -

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L7 and tunneling	10

Database:
- US Patents Full-Text Database
- US Pre-Grant Publication Full-Text Database
- JPO Abstracts Database
- EPO Abstracts Database
- Derwent World Patents Index
- IBM Technical Disclosure Bulletins

Search: L8

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Search History

DATE: Monday, July 28, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=ADJ			
L8	L7 and tunneling	10	L8
L7	L6 and (floating adj gates)	10	L7
L6	L5 and (conductivity adj type)	10	L6
L5	L4 and array	19	L5
L4	L3 and Fowler	21	L4
L3	L2 and (memory adj device)	151	L3
L2	programmable and eraseable	383	L2
L1	programmable adj eraseable	7	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 10 of 10 returned.

☐ 1. Document ID: US 6252799 B1

L8: Entry 1 of 10 File: USPT Jun 26, 2001

US-PAT-NO: 6252799
DOCUMENT-IDENTIFIER: US 6252799 B1

TITLE: Device with embedded flash and EEPROM memories

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6157575 A

L8: Entry 2 of 10 File: USPT Dec 5, 2000

US-PAT-NO: 6157575
DOCUMENT-IDENTIFIER: US 6157575 A

TITLE: Nonvolatile memory device and operating method thereof

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 5953255 A

L8: Entry 3 of 10 File: USPT Sep 14, 1999

US-PAT-NO: 5953255
DOCUMENT-IDENTIFIER: US 5953255 A
** See image for Certificate of Correction **

TITLE: Low voltage, low current hot-hole injection erase and hot-electron programmable flash memory with enhanced endurance

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 4. Document ID: US 5293337 A

L8: Entry 4 of 10 File: USPT Mar 8, 1994

US-PAT-NO: 5293337
DOCUMENT-IDENTIFIER: US 5293337 A
** See image for Certificate of Correction **

TITLE: Electrically erasable programmable read-only memory with electric field decreasing controller

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

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☐ 5. Document ID: US 5168335 A

L8: Entry 5 of 10 File: USPT Dec 1, 1992

US-PAT-NO: 5168335
DOCUMENT-IDENTIFIER: US 5168335 A

TITLE: Electrically programmable, electrically erasable memory array cell with field plate

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

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☐ 6. Document ID: US 5100819 A

L8: Entry 6 of 10 File: USPT Mar 31, 1992

US-PAT-NO: 5100819
DOCUMENT-IDENTIFIER: US 5100819 A

TITLE: Method of making electrically programmable and erasable memory cells with field plate conductor defined drain regions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw. Desc | Image

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☐ 7. Document ID: US 5045489 A

L8: Entry 7 of 10 File: USPT Sep 3, 1991

US-PAT-NO: 5045489
DOCUMENT-IDENTIFIER: US 5045489 A

TITLE: Method of making a high-speed 2-transistor cell for programmable/EEPROM devices with separate read and write transistors

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 8. Document ID: US 4951103 A

L8: Entry 8 of 10 File: USPT Aug 21, 1990

US-PAT-NO: 4951103
DOCUMENT-IDENTIFIER: US 4951103 A

TITLE: Fast, trench isolated, planar flash EEPROMS with silicided bitlines

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 9. Document ID: US 4947222 A

L8: Entry 9 of 10 File: USPT Aug 7, 1990

US-PAT-NO: 4947222
DOCUMENT-IDENTIFIER: US 4947222 A

TITLE: Electrically programmable and erasable memory cells with field plate conductor defined drain regions

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
Draw Desc | Image

☐ 10. Document ID: US 4701776 A

L8: Entry 10 of 10 File: USPT Oct 20, 1987

US-PAT-NO: 4701776
DOCUMENT-IDENTIFIER: US 4701776 A

TITLE: MOS floating gate memory cell and process for fabricating same

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC
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